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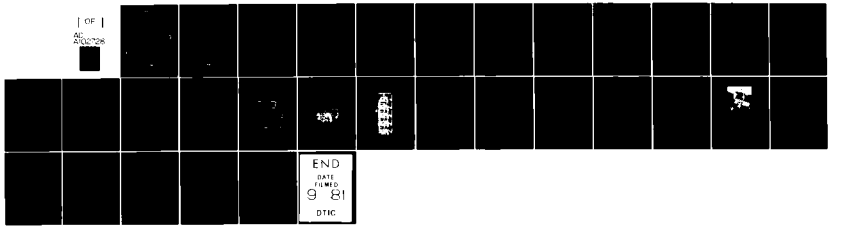

LEVEL II

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FIVE BIT, FIVE GIGASAMPLE TED ANALOG-TO-DIGITAL CONVERTER DEVELOPMENT

INTERIM REPORT

TRW NO. 33730

JUNE 1981

Prepared for

DEPARTMENT OF THE NAVY
OFFICE OF NAVAL RESEARCH
Arlington, Virginia

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DEFENSE AND SPACE SYSTEMS GROUP

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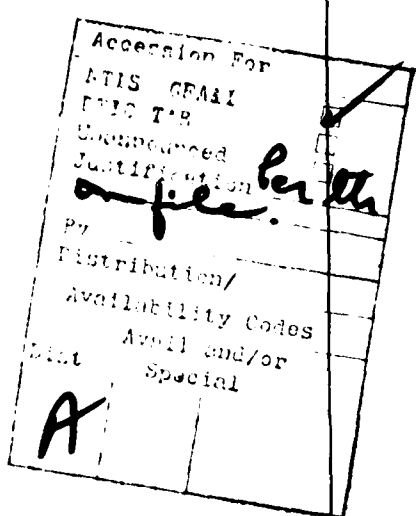
20. ABSTRACT (Continued)

Following this approach an optimized computer-aided design and a complete circuit layout has been accomplished.



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1. INTRODUCTION AND SUMMARY

This report summarizes the work performed by TRW Defense and Space Systems between 1 October 1978 to 31 March 1981 on Contract No. N00014-78-C-0643 for the Office of Naval Research. The objective of this program is the development of a high speed multibit A/D converter based on the monolithic GaAs integrated circuit technology developed at TRW which makes use of gate controlled transferred electron logic devices (TELDs). The GaAs TED/FET A/D bit cell previously developed for the Office of Naval Research under Contract No. SN00014-76-C-0743 has been used as a basic building block. The TELD is a threshold device which can be used in conjunction with a FET comparator circuit in a successive approximation or serial A/D converter. The TELD is capable of very high speed which is the primary motivation for this research.

The original goal for the A/D converter is to demonstrate 5-bit accuracy at 5 Gbps sampling rate. The sampling rate is not at all limited by the TELD function. The TELDs can be designed for operation up to 10 GHz. However, to account for the limited frequency response of the non-optimum FET amplifiers fabricated in optimum TELD materials, the sampling rate of the A/D converter has to be reduced to or below 3 Gbps rate. A simple low-pass design has been adopted for the amplifier/comparator chain which has an upper frequency gain rolloff near 3 GHz. This is an inherent characteristic of the transistor. Since the operation of the cell requires a sampling rate either at the carrier frequency or at a subharmonic of the carrier frequency for proper operation, the sampling rate must be less than 3 gigasamples per second.

A considerable amount of effort has been spent on the circuit modelling and circuit design tasks. A number of design iterations were required to arrive at a satisfactory design. In order to make consideration of the delay path in the matching between the A/D cells manageable a low frequency direct coupling approach was adopted. Following this approach the current design and the complete circuit layout has been done.

Another difficult task encountered was the GaAs material preparation. The active layers for the transferred-electron devices (TEDs) are n-type, doped to a concentration of 1.5 - 3.0 X $10^{16} cm^{-3}$, with an epitaxial thickness

of 1 to 2 μm. These material parameters satisfy the empirical relationship $ND > 1.0 \times 10^{12} cm^2$ required for TED differential negative resistance. The epitaxial material will be thinned in the FET regions to improve the quality of the FET performance. For optimum gain, an $ND^2 > 10^7$ criterion is required. The epitaxial material has to be thinned to 0.2 μm. In addition to the doping-thickness product, the carrier mobility and surface morphology of the vapor phase epitaxial-grown GaAs are also important material parameters to meet these large circuit (approximately 100 x 200 square mils) requirements. Suitable epitaxial GaAs material must be carefully selected for A/D converter chip fabrication. The material must be chosen to satisfy both the transferred-electron logic device (TELD) and field effect transistor (FET) device requirements in a satisfactory manner.

A large number of epitaxial wafers have now been either fully qualified or partially characterized for this contract. Completion of this task is compulsory before starting the circuit fabrication. The most critical part of this development work (both in material and design) has already been completed. The continuing effort will emphasize material characterization, wafer processing, and RF evaluation.

2. HIGH SPEED ANALOG-TO-DIGITAL CONVERTER DESIGN PRINCIPLES

2.1 INTRODUCTION

It is felt that GaAs TED A/D converters have several advantages over their silicon counterparts. The A/D converter is a key element in digital signal processing, as its performance ultimately limits the center frequency and bandwidth to which digital signal processing techniques can be applied. GaAs TED A/D converters can increase both the frequency of operation and the bandwidth over conventional A/D converter designs.

A TED can be considered a very high speed threshold device followed by a short delay line. This makes the TED a particularly useful tool for A/D converter applications. The serial A/D converter, designed to take advantage of the threshold properties of the TEDs, is intended to be an integrated circuit that also uses GaAs field effect transistors (GaAs FETs), bulk GaAs or thin film resistors, and metal oxide metal (MOM) capacitors. A block diagram of the FET-TED A/D converter in serial organization is shown in Figure 2-1. The dashed line encloses one of the bit cells. While there are several ways to organize an A/D converter, the one that takes best advantage of TED properties is the serial organization. This organization is also the most efficient in the number of devices used and the DC power consumed. However, it requires close tolerances in the circuit fabrication.

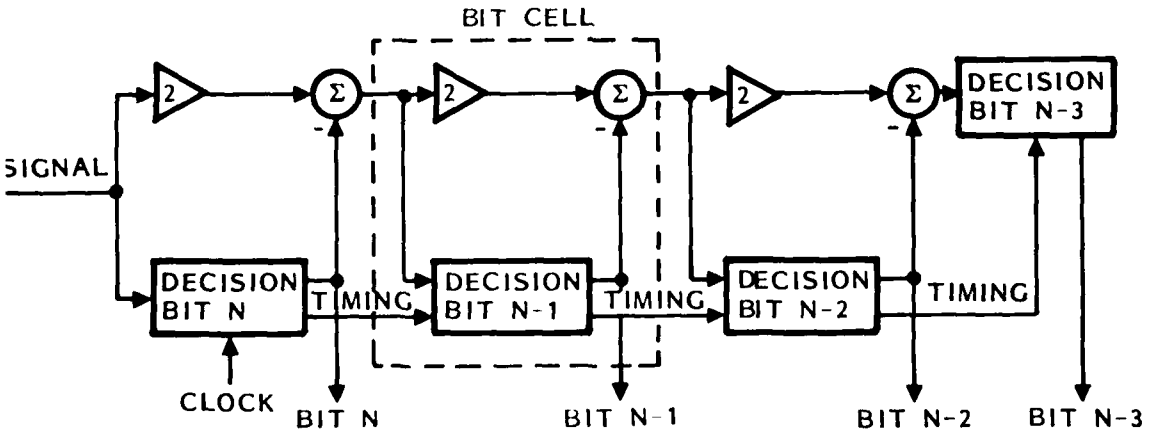

Figure 2-1. Serial, or Successive Approximation, A/D Converter

In pursuing the development of a high speed multiple-bit A/D converter, the design has been based on the monolithic GaAs integrated circuit technologh developed by TRW which includes gate-controlled transfer-electron logic devices (TELDs). The design goal for the A/D converter is 5-bit accuracy at a sampling rate of 3 gigasamples per second in a serial, or successive approximation, A/D converter confiquration

2.2 PRINCIPLES OF SERIAL TYPE A/D DESIGN

Each bit cell of the multiple-bit A/D converter should perform the function illustrated in Figure 2-2.

The amplitude of the RF signal X varies from zero to A. If the amplitude is less than A/2, the digital output from the bit is "0." For $X \geq A/2$, a bit output of "1" occurs. The RF output from the cell which is passed on to the next significant bit cell is $2(X-A/2)$. So if the input X to the most significant cell is A, the output to the next cell and all cells following is also A. If the input to the most significant bit cell is A/2, a "1" will be registered for this cell and the RF output will be "0." The remaining cells will then all register a zero-bit output.

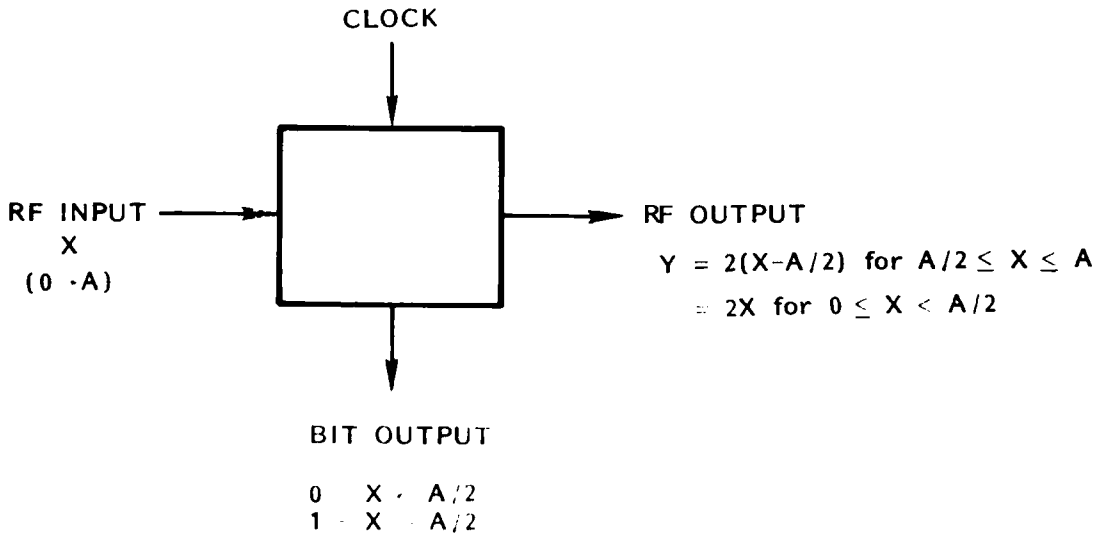

Figure 2-2. Block Diagram of A/D Cell Function

By this algorithm, an A/D converter of as many bits as desired can be constructed. For a 5-bit A/D, 32 quantization levels are available as tabulated in Table 2-1. In this table, the relative RF amplitude levels to each cell are tabulated for relative input levels from 0 to 31. The resulting bit outputs are also tabulated. It is clearly shown that an analog level between zero and the maximum (31) is quantized and represented by a digital binary number output between 0 and 31.

Table 2-1. 5-Bit A/D Quantization Scheme

RF Input (Relative Amplitude) To Cell Number					Bit Output From Cell Number				
1	2	3	4	5	1	2	3	4	5
31	30	28	24	16	1	1	1	1	1
30	28	24	16	0	1	1	1	1	0
29	26	20	8	16	1	1	1	0	1
28	24	16	0	0	1	1	1	0	0
27	22	12	24	16	1	1	0	1	1
26	20	8	16	0	1	1	0	1	0
25	18	4	8	16	1	1	0	0	1
24	16	0	0	0	1	1	0	0	0
23	14	28	24	16	1	0	1	1	1
22	12	24	16	0	1	0	1	1	0
21	10	20	8	16	1	0	1	0	1
20	8	16	0	0	1	0	1	0	0
19	6	12	24	16	1	0	0	1	1
18	4	8	16	0	1	0	0	1	0
17	2	4	8	16	1	0	0	0	1
16	0	0	0	0	1	0	0	0	0
15	30	28	24	16	0	1	1	1	1
14	28	24	16	0	0	1	1	1	0
13	26	20	8	16	0	1	1	0	1
12	24	16	0	0	0	1	1	0	0
11	22	12	24	16	0	1	0	1	1
10	20	8	16	0	0	1	0	1	0
9	18	4	8	16	0	1	0	0	1
8	16	0	0	0	0	1	0	0	0
7	14	28	24	16	0	0	1	1	1
6	12	24	16	0	0	0	1	1	0
5	10	20	8	16	0	0	1	0	1
4	8	16	0	0	0	0	1	0	0
3	6	12	24	16	0	0	0	1	1
2	4	8	16	0	0	0	0	1	0
1	2	4	8	16	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0

The scheme used for realizing the required A/D cell function using FETs and the TELD is shown in the block diagram of Figure 2-3. The RF input signal is provided to a FET amplifier K_1 and TELD 2, the decision block. A clock signal is provided to TELD 1, which acts as a pulse sharpening circuit. The output pulse from TELD 1 provides a clock pulse to TELD 2. When the incoming RF signal is more negative than the TELD trigger threshold when a clock pulse is applied, the TELD 2 will generate an output of peak amplitude V_T. The amplified RF signal K_1 X is then fed, with the TELD output if one exists, to a differential amplification stage K_2. The output from K_2 is the amplified difference of the two input signals $K_2(K_1X-V_T)$.

To satisfy the requirements for the cell design, TELD 2 must trigger on an amplitude of equal to or greater than A/2, where A is the maximum amplitude allowed. Also the product of the two gain factors, K_1 K_2 must equal 2 for the proper signal transfer to the next bit cell. The "phase" of the TELD 2 output, when triggered, must be the same as the output from K_1. Also the magnitude of K_2 V_T must equal A. The actual circuit schematic for the cell has been developed with these constraints in mind.

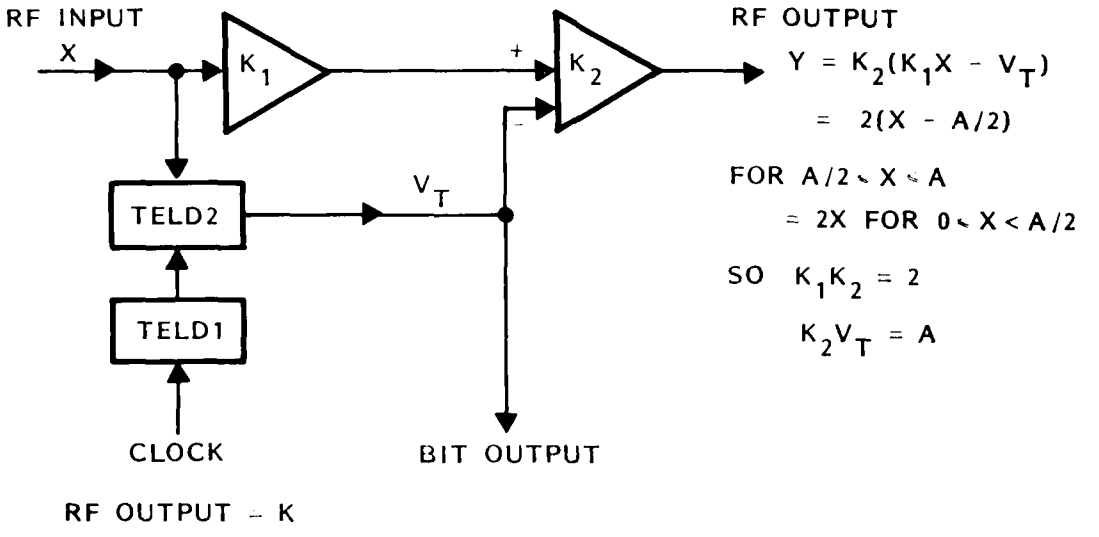

Figure 2-3. TELD A/D Cell Block Diagram

3. TED ANALOG-TO-DIGITAL CONVERTER DESIGN AND LAYOUT

3.1 A/D CELL ELECTRONIC DESIGN

The complete schematic for a single cell of the 5-bit A/D converter is shown in Figure 3-1. The design has been optimized for flat gain as high a frequency as possible while still maintaining sufficient RF gain through the cell. Relating this schematic to the block diagram of Figure 2-3, transistors A and B represents the gain block K_1 and transistors C, D, and E make up the amplifier K_2. The major difficulty confronted in this design was in achieving the desired frequency response in the transistor cascade. First, the upper cutoff frequency f_T for the transistors is relatively low because of the 1-μm gate geometry and non-optimum channel profile. These parameters could not be improved because of constraints of the process technology. Second, the loading of the output of one FET stage by the input impedance of the following stage severely limits the gain bandwidth product of cascaded stages.

The second design problem can be largely overcome by using a buffer in the form of a source follower stage between each common source stage. The common source stage A provides most of the gain in the RF amplifier chain. Stage B is a source follower buffer. The input impedance to B is much higher than that of C so it does not load the output of A as severely as would the capacitive input to another common source stage. Hence B acts as a buffer between A and C. However, the source follower stage has no voltage gain; in fact, there is a small amount of loss.

The differential pair C and D performs the linear differencing amplifier function, with E acting as a current source. The output from the amplifier pair is taken through another source follower buffer G to the next cell. Inclusion of G ensures that the operation of one cell will not be significantly affected by the loading of the next cell.

The TELD section of the circuit presents less of a design problem although there is more uncertainty in predicting the actual performance because TELD behavior varies from wafer to wafer with the present GaAs process control. The decision block, TELD 2, will be triggered by the signal when the amplitude threshold is exceeded and the clock pulse is applied to the second gate. The magnitude of the TELD 2 output voltage V_T times the gain of the comparator K_2 (which includes the loss of the buffer G) must

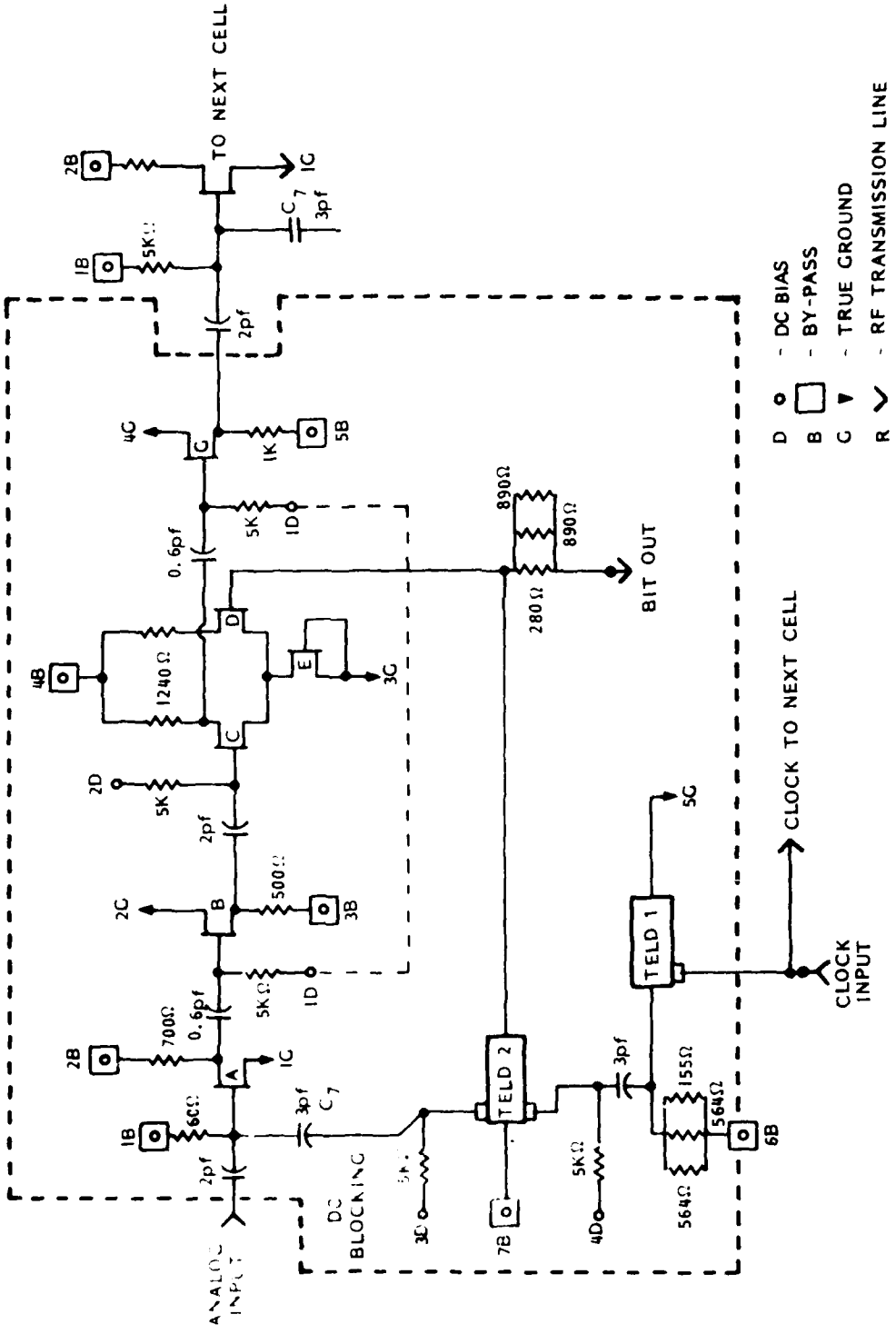

Figure 3-1. Schematic of the 5-Bit, 3-Gigasample/Second A/D Converter

equal A (nominally 0.4 V). There is a limited amount of control of K_2 through dc biasing of the FETs in the pair. The output voltage V_T will depend on the dropback current of the TELD 2 and the load resistance. The dropback current of the TELD can vary significantly from run to run, so load resistance trimming capability has been included to compensate. Three resistors are placed in parallel with the option of laser trimming to remove one or more from the circuit.

A very important aspect of the cell design that is somewhat more subtle is proper phasing and timing. The RF signal impressed on C and the TELD2 signal, when present, impressed on D must be in the same phase for proper action. Now to first order, transistor A inverts the polarity of the amplified RF signal and B does not. Likewise, the TELD 2 inverts the polarity from input to output. However, there is additional phase delay in the RF amplifier chain owing to capacitive loading, etc. There is also compensating delay in the TELD 2 branch caused by domain buildup time, and capacitive loading of the TELD 2 output by the input of D. An estimate of the phase delay in the TELD 2 branch was made by modeling the TELD as a voltage-controlled current generator with a built-in time delay between impressed voltage and output current. Based on this estimate and the phase delay calculated for the amplifier chain from a SPICE analysis, the phase delays cancel one another to first order. The time delays caused by finite length interconnects between the circuit elements have been taken into consideration.

3.2 FIVE-BIT FET/TED A/D CONVERTER LAYOUT

The schematic diagram of a single cell of the 5-bit A/D converter is shown in Figure 3-1. In this optimized design, the capacitors are reduced considerably from the initial COMPACT runs. The purpose of this is to minimize the unnecessary circuit capacitance without sacrificing the RF performance. One of the major yield-loss factors in the present GaAs IC process is the dielectric pinhole defects. The direct advantage of minimizing circuit capacitance is to increase wafer fabrication yield. The standard capacitance value of 0.1 pf/square mil has been commonly used in TRW's standard process. The average sheet resistance value of bulk GaAs epitaxial resistors of 425 Ω/square has been adopted for the layout of the A/D converter circuit. The layout of a single cell of the A/D converter is shown

in Figure 3.2. A complete single bit A/D converter including bonding pads and interconnects is shown in Figure 3-3. A complete five cell pattern has been generated from the single cell layout. Special consideration has been given to the situation of an RF input signal propagating through the FET amplifier's chain to be matched in phase with the signal arriving at the comparator block from the TELD decision function. The RF delay lines in the layout of each cell have been readjusted to equalize the phase in both signal paths accounting for the interconnect lengths. The RF clock line has been examined to make sure the clock signal for each cell is in proper phase with the RF signal propagation from cell to cell. The final complete layout (Figure 3-4) is generated for mask making.

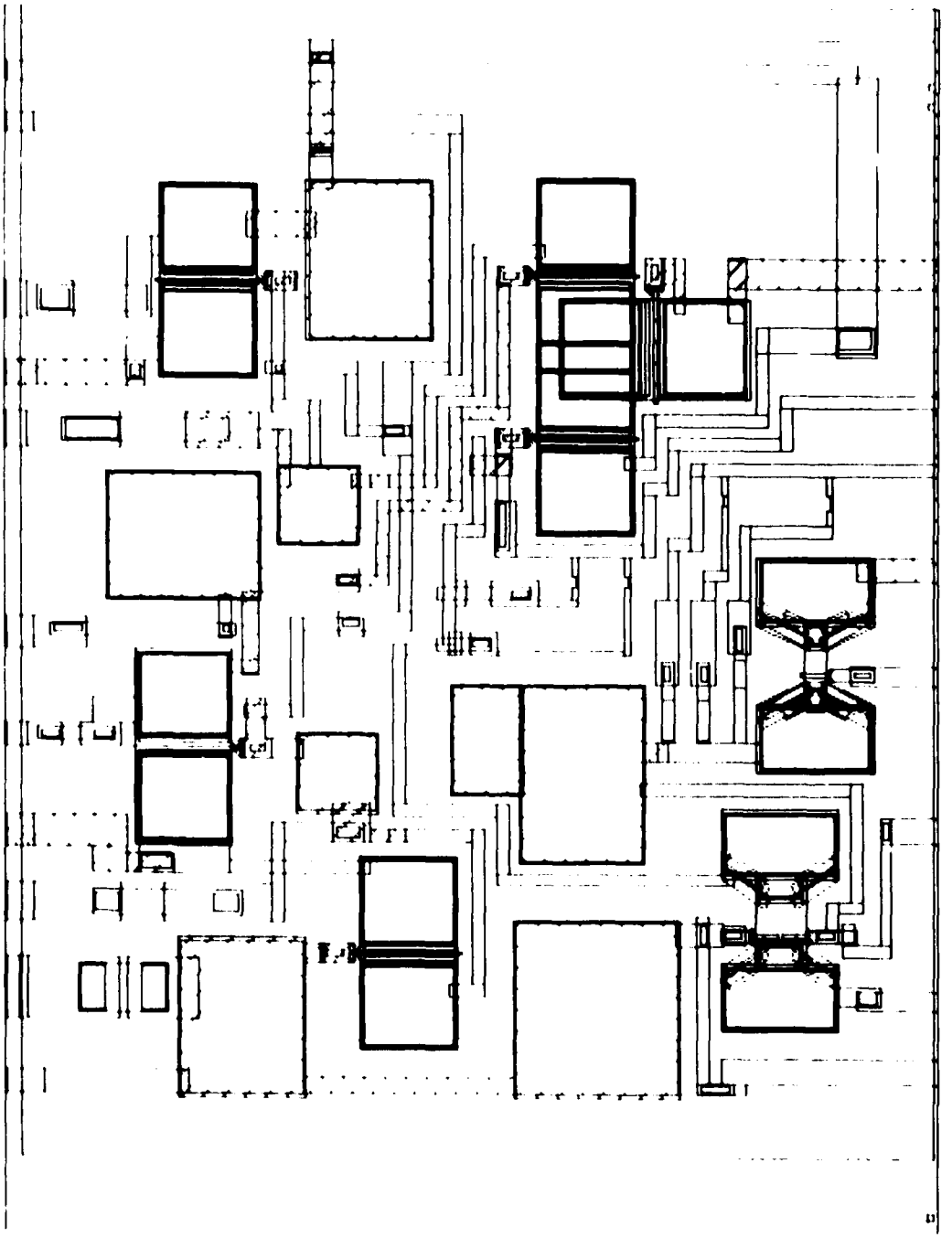

Figure 3-2. Final Layout of a Single Cell of A/D Converter

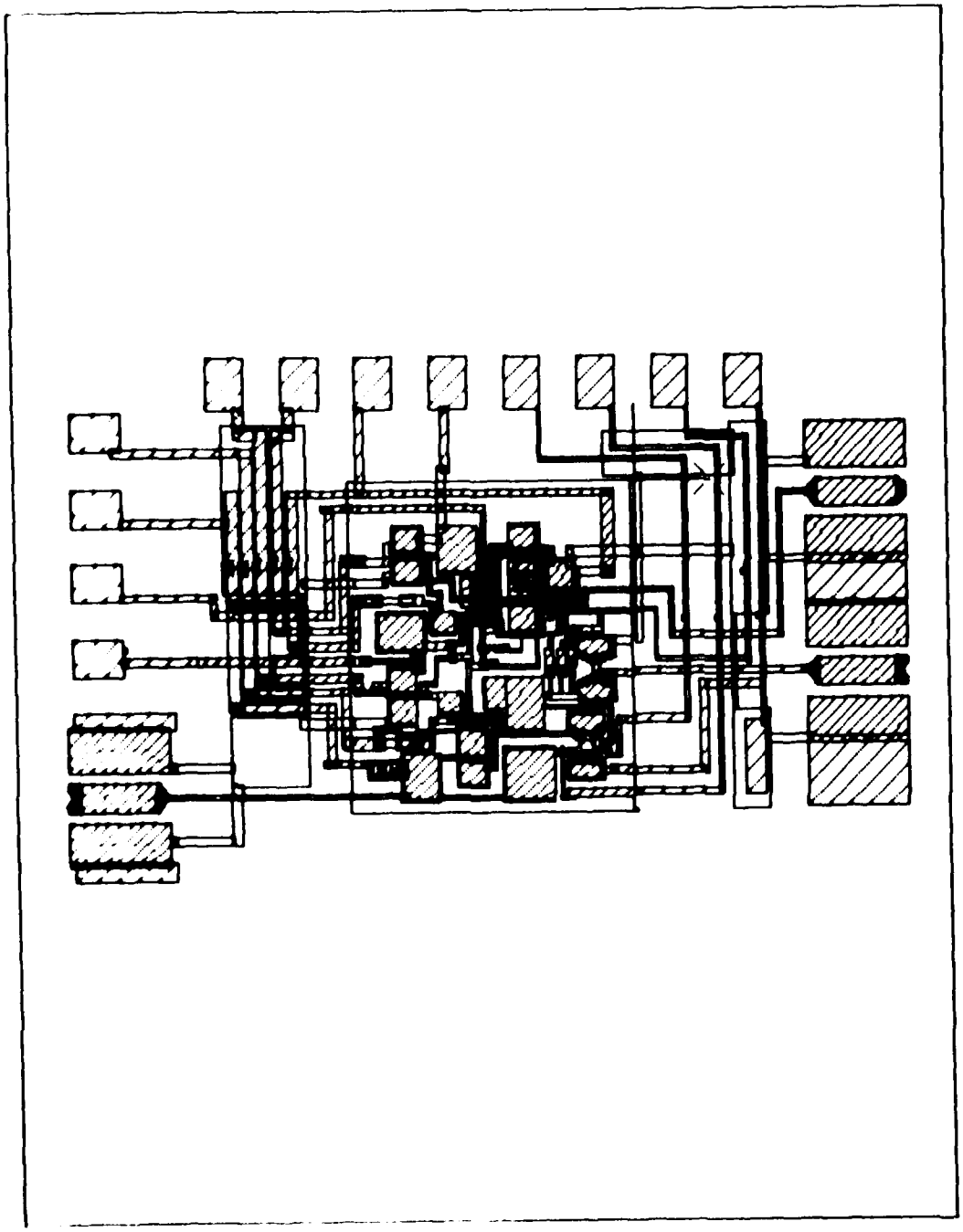

Figure 3-3. A Complete Single Bit A/D Converter

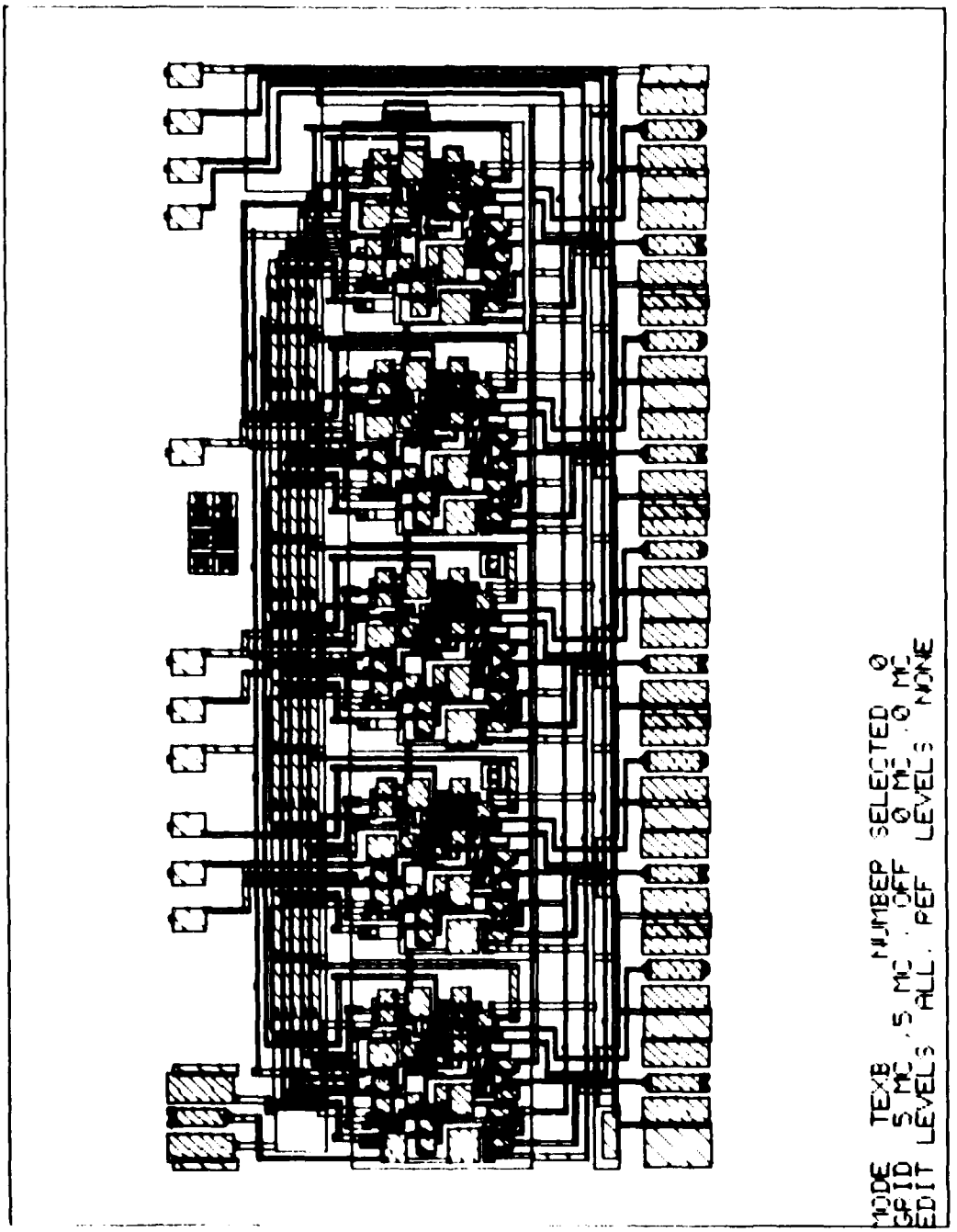

Figure 3-4. Complete Layout of a Five-Bit A/D Converter

4. TED MATERIALS AND I.C. PROCESSING

This section describes the materials and processes to be employed in fabricating the 5-bit A/D converter circuit for this contract (N00014-78-C-0643). The existing technology will be used for TEDs, FETs, and passive elements. Epitaxial material has been grown for use in these circuits. This material is optimum for TEDs, but must be selectively etched to optimize for FETs.

4.1 GaAs MATERIALS FOR TED AND FET INTEGRATED CIRCUITS

The success of fabricating any IC depends on the properties of the starting material. This is especially true for GaAs ICs. The properties of GaAs epitaxial materials can vary extensively during epitaxial growth. The active layers are deposited epitaxially on GaAs semi-insulating substrates. The properties of both bulk GaAs crystal and epitaxial layers affect the final device performance in the circuit. Bulk properties of the substrate materials such as dislocation density, dopant concentration, and mobility have been controlled by working closely with the substrate suppliers. TRW uses two sources at present: materials grown by Horizontal Bridgman technique from Crystal Specialties, and Czochralski from MRI.

The epitaxial material is grown in a commercially designed, vapor phase vertical system with AsH_3, HCl, and GaAs the principal reactants. Epitaxial material from this system has been successfully used to fabricate discrete TEDs, MESFETs, millimeter wave mixers, and small-scale integrated circuits.

These wafers employ undoped buffer layers prior to the deposition of the doped active layer. The active layer is doped to a range of $1 - 5 \times 10^{16}$ cm^{-3} using H_2S source for the sulfur dopant.

Ion-implanted TEDs have also been developed at TRW. They represent a viable alternate to the mesa process. The use of ion-implantation permits selectively implanting the FET and TED regions separately to permit optimization of each.

The active layers for the TEDs are n-type, doped to a concentration of $1.5 - 3.0 \times 10^{16}$ cm^{-3}, with an epitaxial thickness of $1 - 2$ μm. These material parameters satisfy the empirical relationship $ND > 1.0 \times 10^{12}$ cm^2 required for TED devices. The epitaxial material will be thinned to 0.2 μm

in the FET regions to improve the quality of the FET performance. For optimum gain, an $ND^2 \quad 10^7$ criterion is required. The epitaxial layer has to be thinned to 0.2 μm in these areas. The program plan is to use the epitaxial layer with the TED parameters and etch back in the FET regions for optimum pinchoff voltage. Approximately 20 wafers have been deposited with epitaxial layers and will be used for this program. These wafers will be characterized and used to process the ICs.

4.2 INTEGRATED CIRCUIT PROCESSING

The IC process described as an "epitaxial mesa process" will employ the standard ohmic contacts, rectifying contacts, and passive elements developed over the past five years. The ohmic contacts are AuGeNi alloyed at 420°C to give a specific contact resistivity of about 3×10^{-5} Ω-cm^2. When N+ implants are used in the contact region, the specific resistance reduces to 10^{-6}-10^{-7} Ω-cm^2. Gates for the rectifying contacts are CrPtAu. Both metals are deposited and delineated using a photoresist liftoff technique.

Two passive elements to be used in these circuits are thin film MOM capacitors and bulk resistors. The bottom plate of the capacitor is deposited in the same deposition as the gate metal. The dielectric in the capacitor is SiO_2 (low temperature Silox) and the top plate metallization uses TiAl as the final bond and interconnect metal. Resistors for the circuits will be bulk GaAs resistors, with gross trimming provided by removing resistors from parallel paths in the circuit.

The process flow diagram is shown in Figure 4-1.

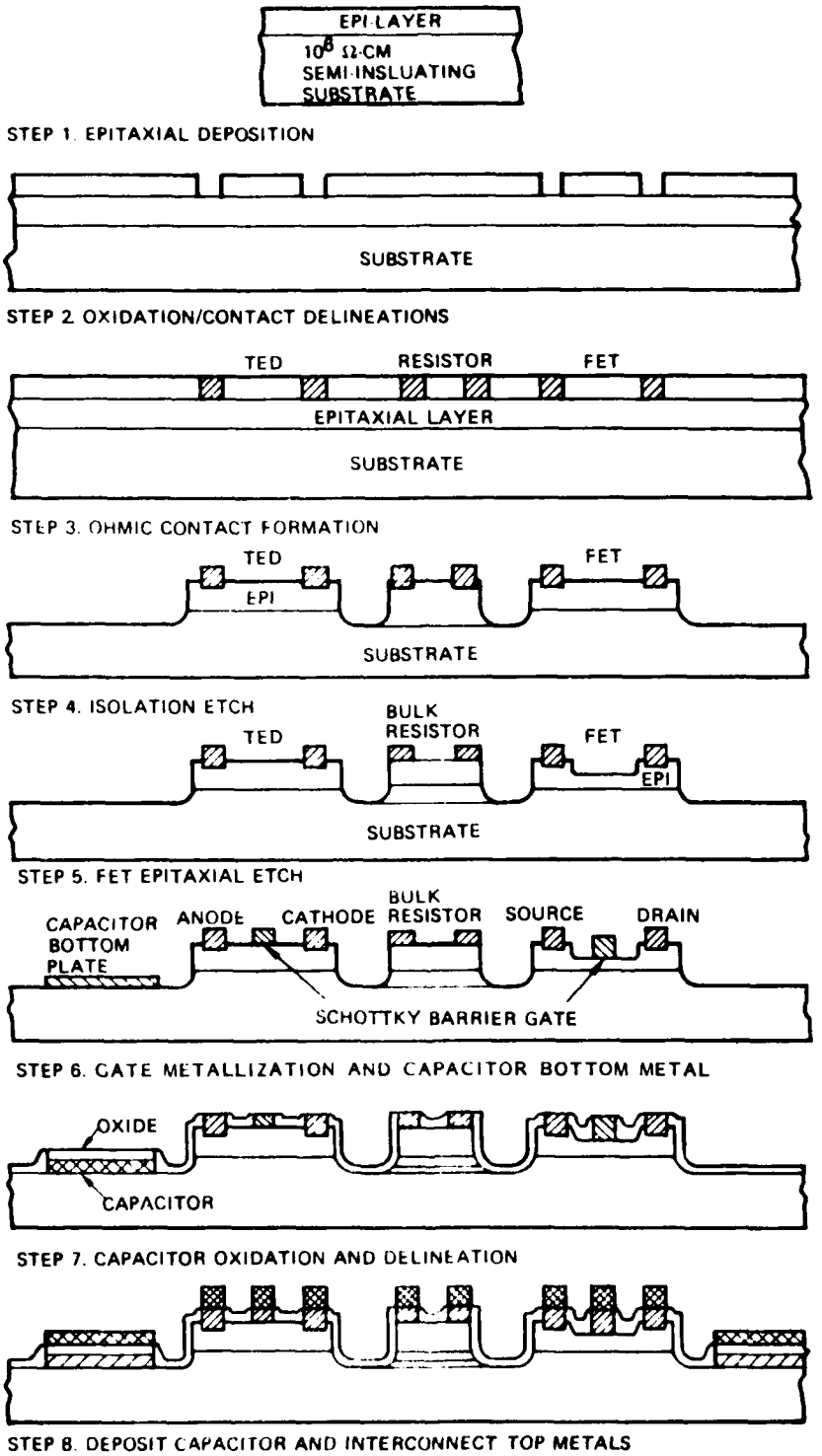

Figure 4-1. Steps in Processing TED-FET Integrated Circuits

5. A/D CONVERTER TEST AND EVALUATION PLAN

5.1 TEST FIXTURE DESIGN AND ASSEMBLY

The two most common types of transmission media used in microwave ICs to interface with the outside world are microstrip lines and coplanar lines. The impedance of a microstrip transmission line is determined by the dielectric constant of the substrate material, the width of the surface conductor, and the separation of the surface conductor and its ground plane. For a given dielectric thickness of a certain substrate material, the width of the surface conductor is fixed for the specific impedance one requires. For example, a 50-Ω transmission line of a 25-mil alumina substrate (relative dielectric constant of 11.0) requires approximately a 25-mil-width of the surface conductor. However, since the width of the chip bonding area on GaAs is on the order of 2 to 3 mils and is separated by 10 to 15 mils, microstrip lines are incompatible for this case. Furthermore, microstrip lines having such proximity are subject to field interference and crosstalk from the other parts of the circuit. The problem of interfacing to the test fixtures, which may be made of different materials (such as alumina) from the actual IC and of different thickness is difficult to solve by using microstrip techniques.

The use of coplanar lines offers a convenient solution to these problems. A coplanar transmission line consists of a narrow strip with two ground planes running adjacent and parallel to the strip on the same side of a substrate. The coplanar configuration is especially convenient for connecting external shunt elements such as microwave diodes, resistors, and capacitors.

The impedance of a coplanar line can be kept constant and independent of the actual width of the line as long as the ratio between line width and parallel ground plane spacing remain constant. This means that a line of 50 Ω or any other impedance value can be fabricated with equal facility, using a large or small physical size. This property can be used to taper the transitions from one substrate to another without ever deviating from a constant impedance.

TRW has developed a computational method for solving for coplanar line parameters based on a finite difference method with a network elimination technique. The calculated impedance for coplanar lines using this technique is shown in Figure 5-1.

In designing RF test fixtures for GaAs ICs, TRW has adopted the approach of using a tapered coplanar line to provide the RF feed from the SMA connector interface to the chip. The dc lines are usually supplied by high impedance microstrip. A typical test fixture design used to test GaAs TED A/D converters is shown in Figure 5-2.

5.2 TEST PROCEDURE AND SETUP

A single bit A/D cell and dual-gate TEDs have been added to the mask design. The dual-gate TEDs will be used for process and material characterization. The testing of single cell of the A/D converter will help to determine the following parameters:

1) Approximate bias conditions required for each cell

2) Proper bias adjustment for adjusting gain within the cell to provide the necessary gain - a factor of 2 for each cell

3) An estimate of the bandwidth that can be obtained.

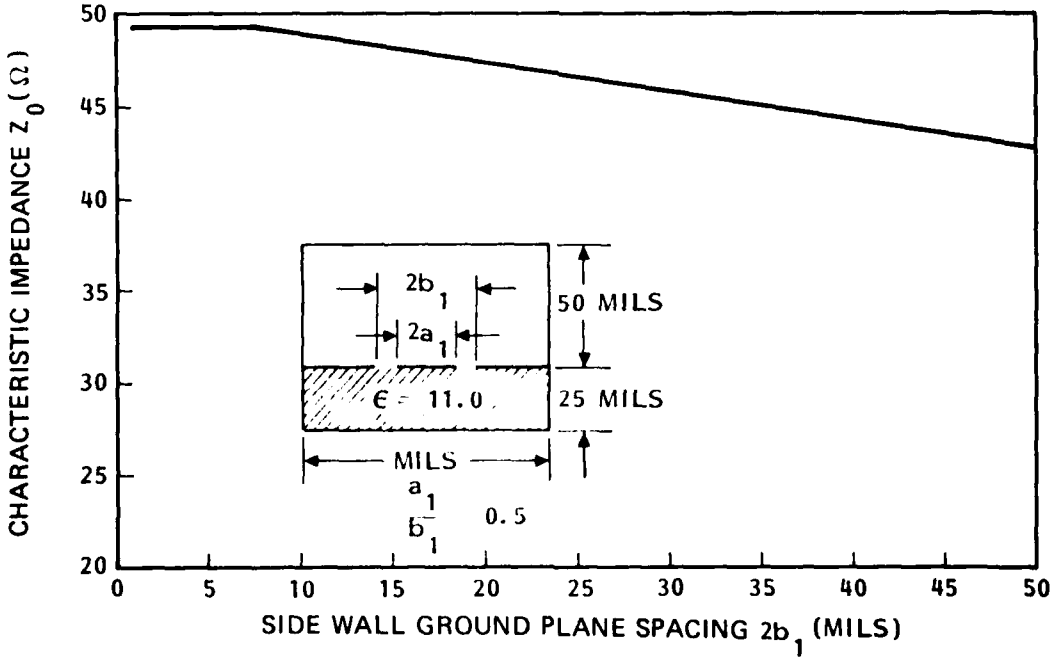

Figure 5-1. Coplanar Transmission Line Impedance Characteristic

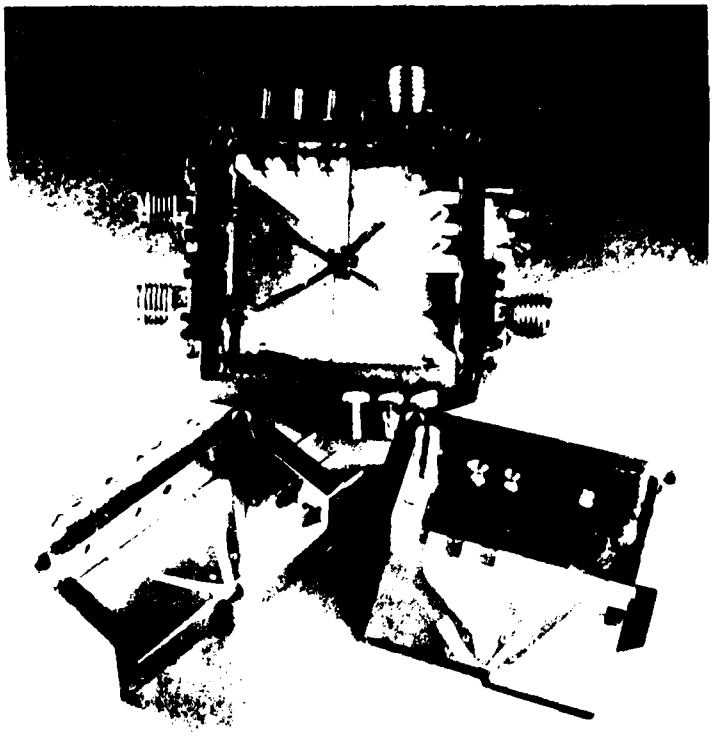

Figure 5-2. Photograph of Test Fixture Assembly

The serial design of this 5-bit A/D converter is based on two basic building blocks in the cell: a FET differential amplifier and a dual-gate TED as a decision block. The sampling process in the A/D circuit design is carried out by the FET and TED combination. The circuit design requires that the analog signal be translated up in frequency. The circuit can be tested by using a 3-GHz CW signal and varying its power. Referring to Figure 3-1, one gate of TELD2 receives the clock pulse from TELD1. A sinusoidal clock signal is provided to TELD1, which acts as a pulse-sharpening circuit. The output pulse from the TELD has a fast risetime, reducing the false triggering, hence reducing bit errors at the output of the cell. The other gate of TELD2 receives the RF input signal.

The digitizing of the analog signal takes place as follows. The triggering of TELD2 produces a pulse, after a small delay, at the bit output port of the cell. This takes place when the analog input signal amplitude is above the midrange input level of the cell. When the analog input is less

than the midrange input level, the bit output is a digital "0." When the analog input is greater than the midrange level, the bit output is a digital "1."

For a serial organization of multiple-bit A/D cells, the gain and summation operations of each cell are critical to the proper operation of a serial A/D converter. The summation and feed-forward operation of this cell are accomplished in the FET differential pair. (The A/D cell circuit samples an analog signal, digitizes that signal, and supplies a feed-forward signal to allow the cascading of single cells to form a multiple-bit A/D converter.)

The evaluation of the single and 5-bit A/D chips can be performed using the system shown in Figure 5-3. The input to the chip consists of an RF carrier which can be amplitude-modulated and a clock signal which can be properly synchronized. The initial test will be to bias the cells properly and apply a cw signal of sufficient amplitude to produce a high or "1" state in all cells. The RF amplitude required to accomplish this is "A," the maximum allowed input amplitude to the chip. The input amplitude will then be reduced slowly to step the A/D through the proper output sequence following the truth table of Table 2-1. This test will ensure that the threshold of each sampling TED is set properly and that the proper signal transfer is made from cell to cell.

Once the thresholds are set properly, the bandwidth of the A/D will be evaluated. As the frequency of the amplitude modulation on the input RF carrier is increased, the input signal spectrum is spread. Because of the limited bandwidth of the FET amplifying chain, the propagated signal will be distorted causing bit errors to occur. This condition will occur first in the least significant bit and progress to the more significant bit as the input bandwidth increases further. The bandwidth of the A/D will be determined as a function of bit resolution as follows:

1) The input amplitude will be set at a suitable level and the bit outputs will be noted.

2) A slowly varying AM modulation will be applied with the peak amplitude being the same as in step 1. This will cause a bit pattern output from each cell which reflects the time varying input amplitude.

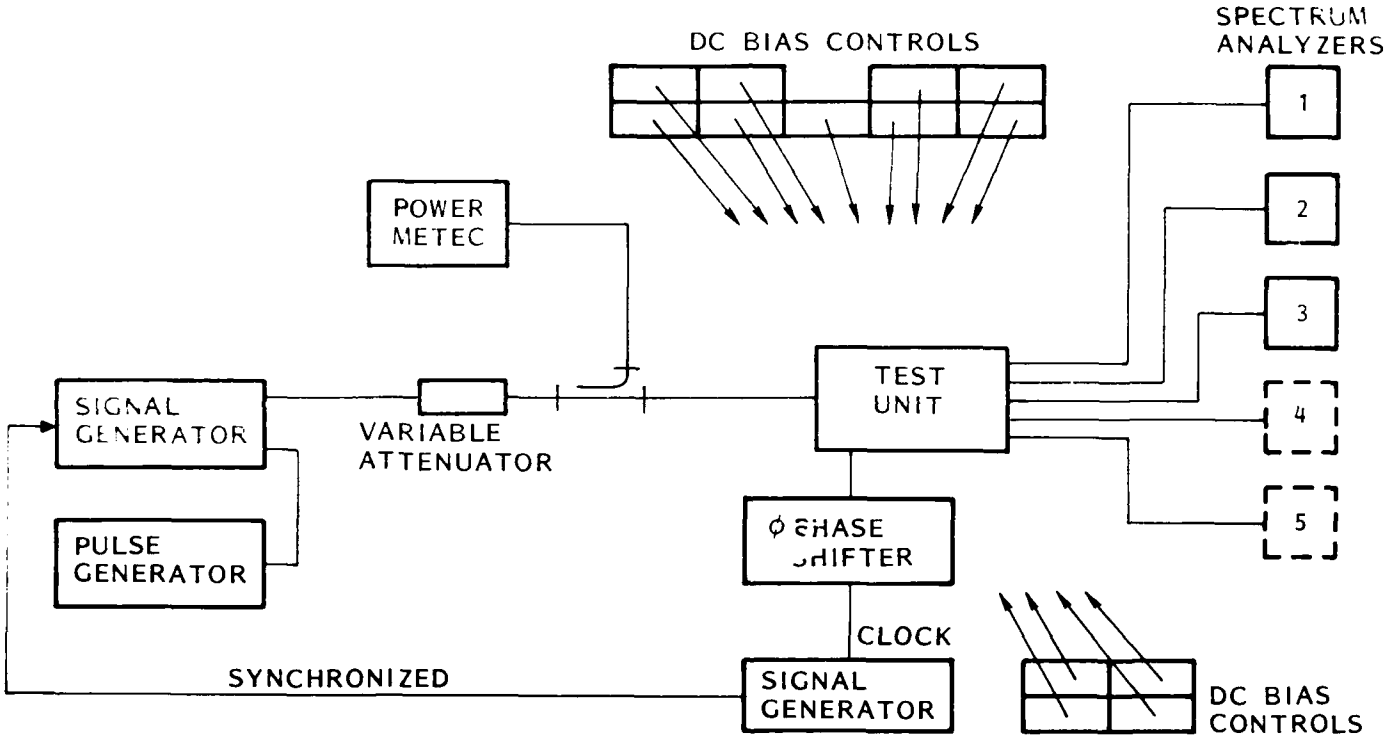

Figure 5-3. 5-Bit A/D Converter Test Setup

3) Holding the modulation index constant, the frequency of the AM modulation will be increased until the bit output pattern for the least significant bit cell becomes erratic. The frequency of the AM modulation at this point determines the maximum bandwidth for 5-bit resolution.

4) The AM modulation frequency will be increased further to determine the bandwidth for 4-, 3- and 2-bit resolutions.

The two tests described will fully characterize the performance of the TED-based A/D converter chip.

6. PLANS FOR COMPLETION

A high speed 5-bit A/D converter design and layout has been completed which has a relatively high probability of being successfully implemented with TRW's standard GaAs IC fabrication techniques. The design has been made as simple as possible while still demonstrating the feasibility of using a TELD for performing the RF analog-to-digital conversion with 5-bit resolution. Based on the result from numerous iterations between SPICE and COMPACT modelling, a design of optimized overall voltage gain for the amplifier/comparator chain was defined. The final layout of this design has been generated. The plans for completion of this contract are:

- Final check of the layout and bonding pads
- Fabrication of mask sets
- Characterization and selection of GaAs epi materials; if necessary additional GaAs epi material will be prepared
- I.C. wafer processing and D.C. probing
- A/D converter test fixture design and fabrication
- Complete A/D converter evaluation
- Reporting (bimonthly and final report)
- Demonstration hardware delivery

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